



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,854	06/02/2004	Tzyh-Cheang Lee	NAUP0576USA	3853
27765	7590	09/09/2004	EXAMINER	
NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)			WILSON, SCOTT R	
P.O. BOX 506			ART UNIT	
MERRIFIELD, VA 22116			PAPER NUMBER	
			2826	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/709,854

Applicant(s)

LEE ET AL.

Examiner

Scott R. Wilson

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>6/2/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Haspeslagh. As to claim 1, Haspeslagh, Figure 5, discloses an electrically programmable non-volatile memory cell comprising a semiconductor substrate of first conductivity type, a pair of spaced apart source/drain regions (13) and (14) defined on said semiconductor substrate (paragraph 0051), a channel region (18) between said source/drain regions (paragraph 0060), a first dielectric layer (4)(Figure 2f, paragraph 0057) disposed on said source/drain regions, an assistant gate (7) stacked on said first dielectric layer, wherein said assistant gate has a top surface and sidewalls, a second dielectric layer (17)(Figure 2f, paragraph 0057) comprising a charge-trapping layer uniformly disposed on said top surface and sidewalls of said assistant gate and disposed on said channel region, wherein said second dielectric layer produces a recessed trough (11) between said source/drain regions, and a conductive gate material filling said recessed trough (11)(paragraph 0057) for controlling said channel region, wherein, in operation, said assistant gate is biased to a voltage V_i that is sufficient to induce a corresponding inversion region of second conductivity type in said semiconductor substrate (paragraph 0100), and wherein said inversion region of second conductivity type functions as a source/drain of said electrically programmable non-volatile memory cell (paragraph 0100).

As to claim 2, Haspeslagh discloses (paragraph 0054) that the first dielectric layer (4) is made of silicon dioxide.

As to claim 3, Haspeslagh discloses (paragraph 0054) that the silicon dioxide layer is thermally grown.

Art Unit: 2826

As to claim 4, Haspeslagh discloses (paragraph 0057) that the second dielectric layer is a tri-layer.

As to claim 5, Haspeslagh discloses (paragraph 0057) that the second dielectric layer is an ONO tri-layer, said charge-trapping layer is a silicon nitride layer (9) sandwiched between a bottom oxide layer (8) and a top oxide layer (10).

As to claim 6, applicants prior art (Yang et al.) discloses (col. 5, line 51) that the charge-trapping layer may be embodied as an oxide/nitride bilayer dielectric.

As to claim 7, Haspeslagh discloses (paragraph 0053) that the assistant gate (7) is made of polysilicon.

As to claim 8, Haspeslagh discloses (paragraph 0057) that the conductive gate material (11) comprises polysilicon.

As to claim 9, Haspeslagh discloses (paragraph 0057) that, although the conductive gate material (11) is taught to be polysilicon, the teaching of polysilicon is only an example, therefore other conductors, such as metal, are within the scope of the disclosure.

As to claim 10, Haspeslagh, Figure 4, discloses that the inversion region of second conductivity type is electrically connected to a pickup well (B_1)(paragraph 0062) that is formed in said semiconductor substrate at one end of the assistant gate, and which is biased to a bitline voltage.

Claims 11-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Haspeslagh. As to claim 11, Haspeslagh, Figure 5, discloses an electrically programmable non-volatile memory cell comprising a semiconductor substrate, a pair of spaced apart source/drain regions (13) and (14) defined on said semiconductor substrate (paragraph 0051), a channel region (18) between said source/drain regions (paragraph 0060), a first dielectric layer (4)(Figure 2f, paragraph 0057) disposed on said source/drain regions, an assistant gate (7) stacked on said first dielectric layer, wherein said assistant gate has a top surface and sidewalls, a second dielectric layer (17)(Figure 2f, paragraph 0057) comprising a charge-trapping layer uniformly disposed on said top surface and sidewalls of said assistant gate and disposed on said channel region, wherein said second dielectric layer provides a recessed

Art Unit: 2826

trough (11) between said source/drain regions, and a conductive gate material filling said recessed trough (11)(paragraph 0057).

As to claim 12, Haspeslagh discloses that, in operation, said assistant gate is biased to a voltage V_i that is sufficient to induce a corresponding inversion region in said semiconductor substrate (paragraph 0100), and wherein said inversion region functions as a source/drain of said electrically programmable non-volatile memory cell (paragraph 0100).

As to claim 13, Haspeslagh discloses (paragraph 0054) that the first dielectric layer (4) is made of silicon dioxide.

As to claim 14, Haspeslagh discloses (paragraph 0057) that the second dielectric layer is an ONO tri-layer, said charge-trapping layer is a silicon nitride layer (9) sandwiched between a bottom oxide layer (8) and a top oxide layer (10).

As to claim 15, Haspeslagh discloses (paragraph 0053) that the assistant gate (7) is made of polysilicon.

As to claim 16, Haspeslagh discloses (paragraph 0057) that the conductive gate material (11) comprises polysilicon.

As to claim 17, Haspeslagh discloses (paragraph 0057) that, although the conductive gate material (11) is taught to be polysilicon, the teaching of polysilicon is only an example, therefore other conductors, such as metal, are within the scope of the disclosure.

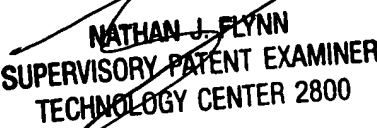
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2826

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
September 1, 2004


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800